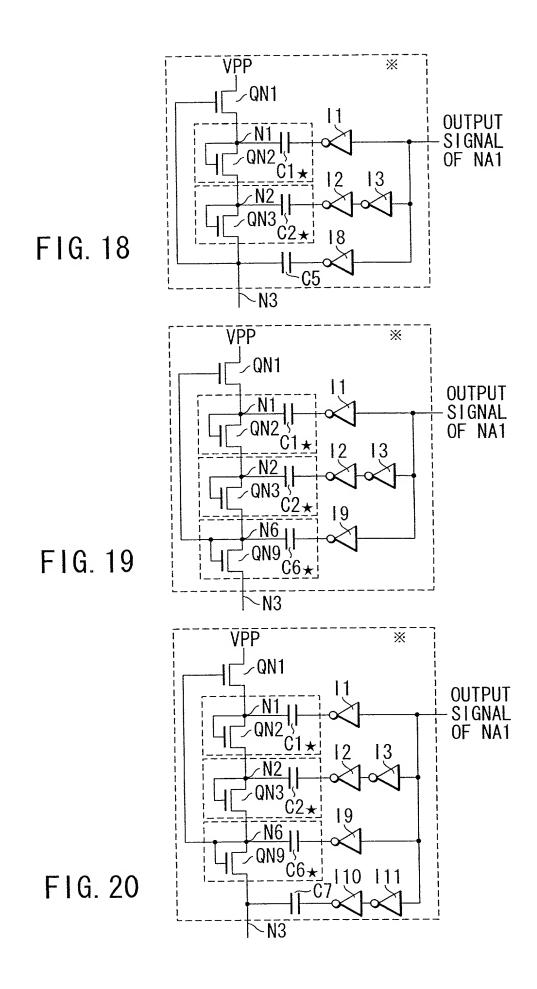
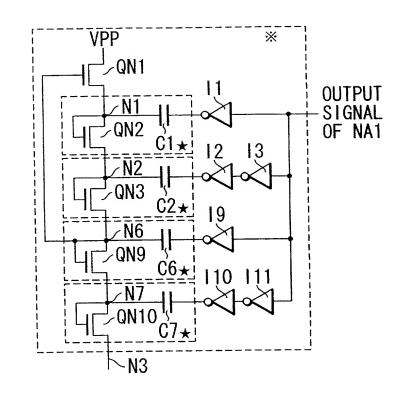


VPP \sim QN1 \sim QN1 \sim QN2 \sim QN2 \sim QN2 \sim QN2 \sim QN2 \sim QN2 \sim QN3 \sim QN3 \sim QN3 \sim QN9 \sim QN9

N3

FIG. 17





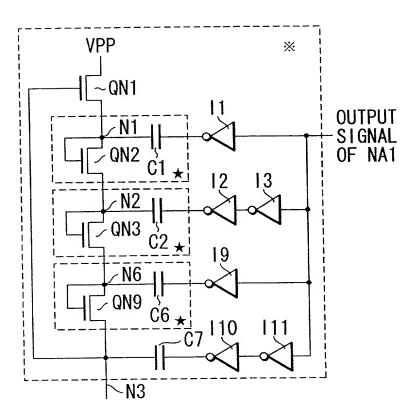
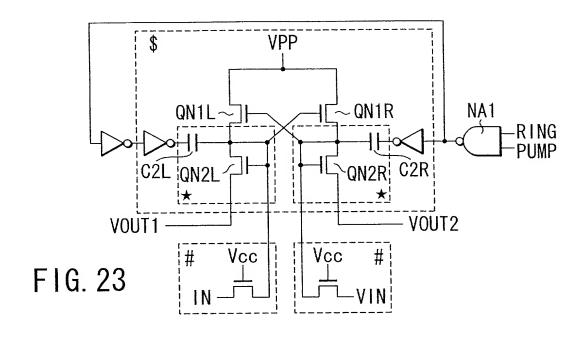
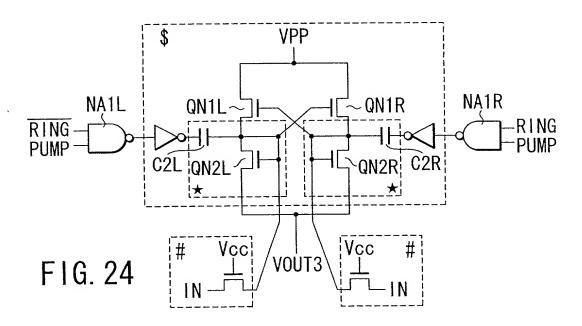


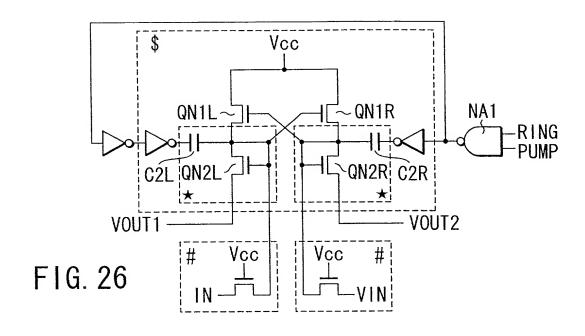
FIG. 22

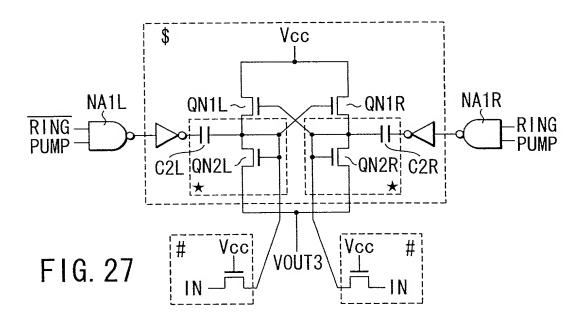
FIG. 21

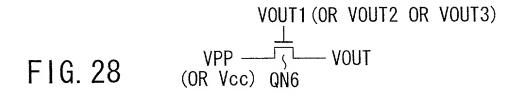


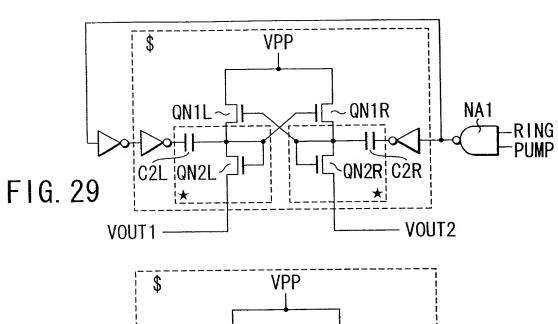


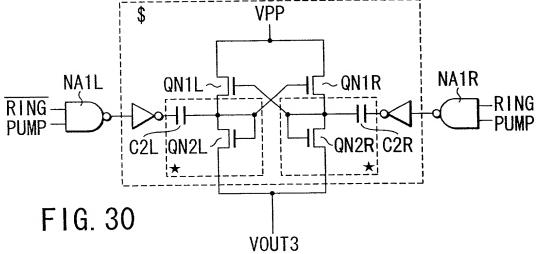
VOUT1 (OR VOUT2 OR VOUT3) $\begin{array}{c} VPP & \stackrel{}{-} \checkmark \\ VPP & \stackrel{}{-} \checkmark \\ VOUT \\ (OR\ Vcc)\ QN6 \end{array}$

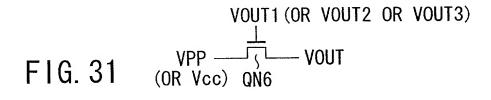


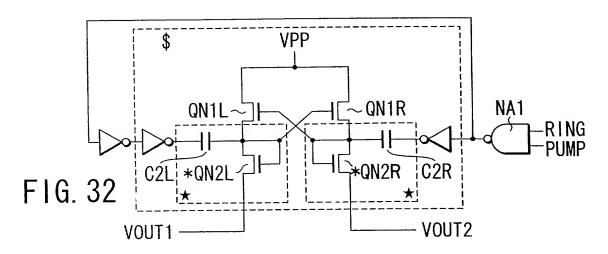


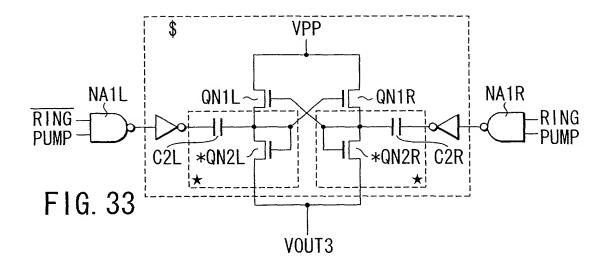


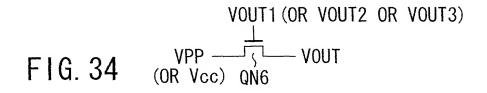


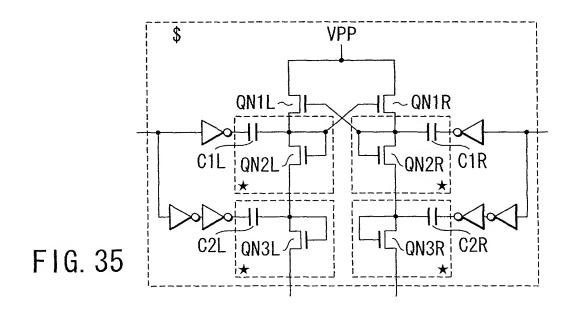


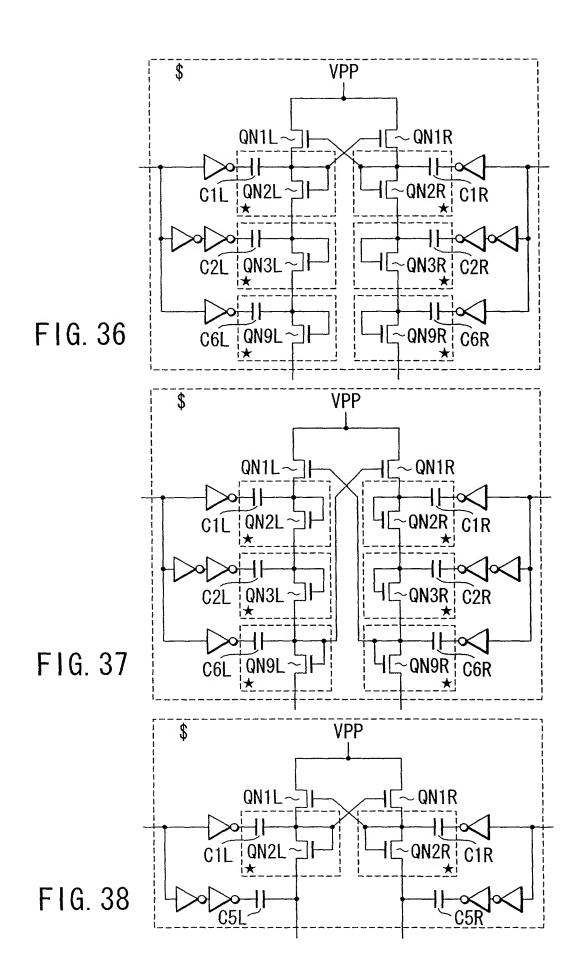


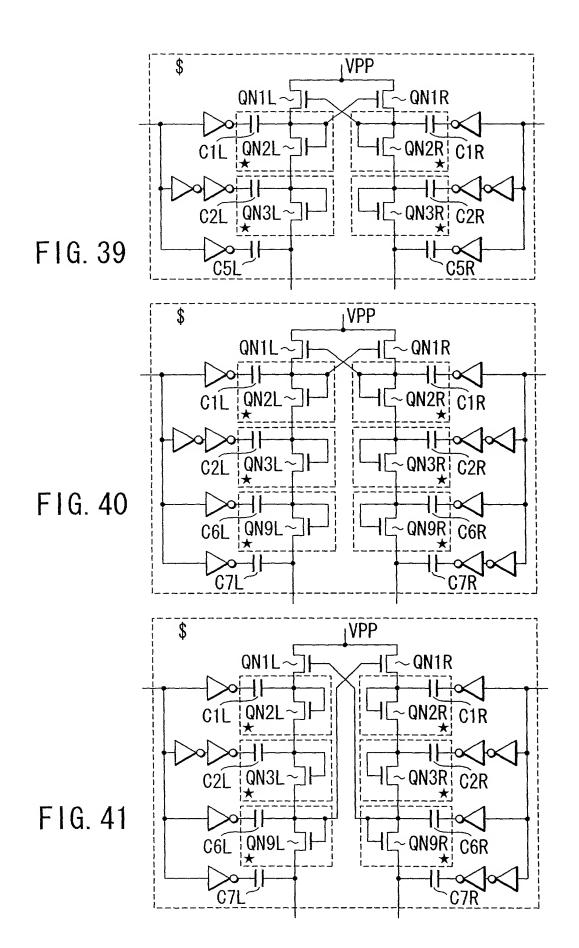


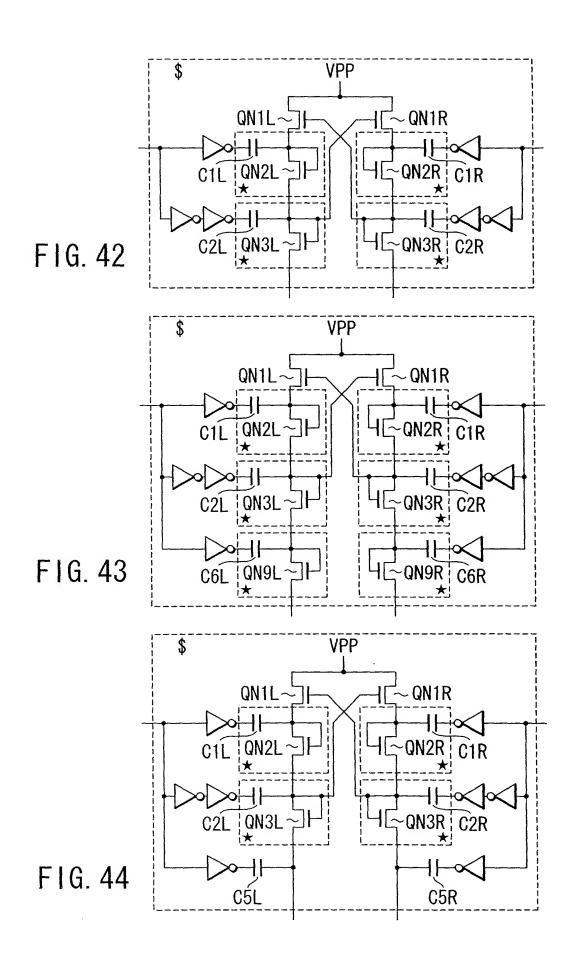


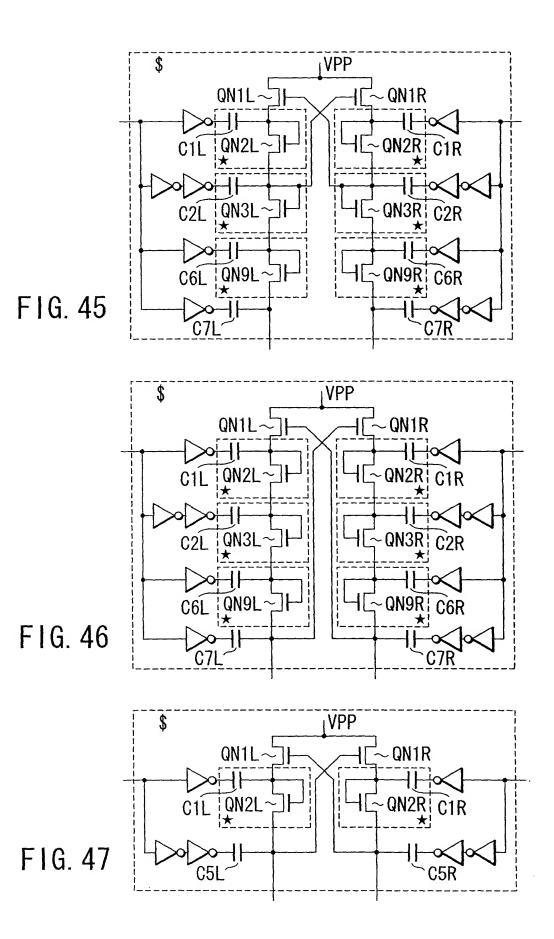


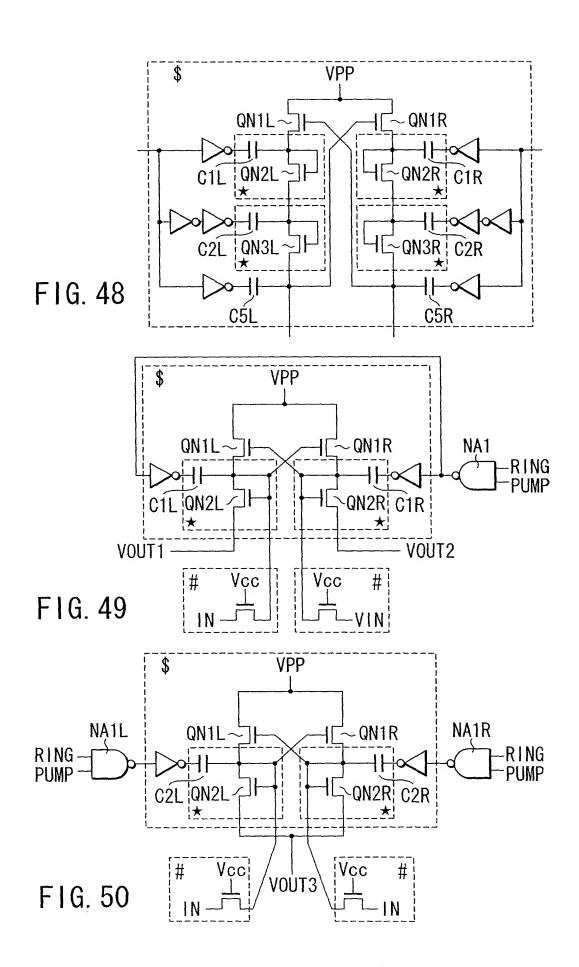


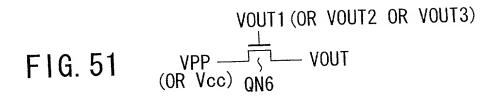












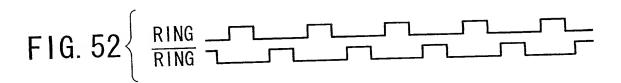
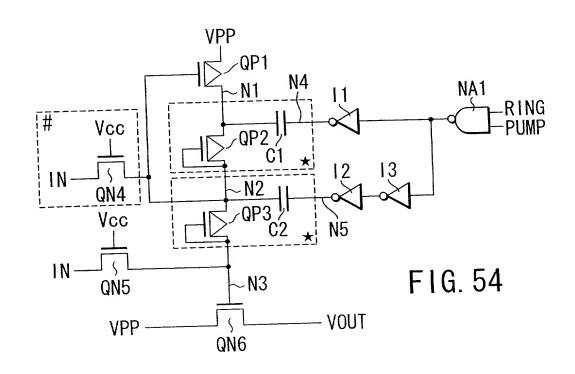


FIG. 53
$$\left\{ \begin{array}{l} \frac{RING}{RING} \\ \hline \end{array} \right.$$



, A . W

